

S/N 09/893,023

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank O'Mahony et al.

Examiner: Unknown

Serial No.: 09/893,023

Group Art Unit: 2812

Filed: June 27, 2001

Docket: 884.405US1

LOW LOSS INTERCONNECT STRUCTURE FOR USE IN MICROELECTRONIC
CIRCUITS

SEP 16 2002

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representatives at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

FRANK O'MAHONY ET AL.

By their Representatives,

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Date

9-11-02

By

Dana B. LeMoine
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 11 day of September, 2002.

Jane F. Brockschink
Name

Signature